Murali Krishna L

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EDUCATION

Rajalakshmi Engineering College — Tamil Nadu, India
Bachelor of Engineering, Electronics and Communication; CGPA: 8.3 — **May 2025**

Don Bosco Matriculation Higher Secondary School — Tamil Nadu, India
SSLC and HSC, State Board; SSLC: 82.4% and HSC: 87.5% — **May 2021**

SKILLS SUMMARY

- **RTL Design:** Verilog HDL, SystemVerilog, FSM Design, RTL-level pipelining, ALU, MUX, RAM, IO modules
- **Verification:** Testbench development, SystemVerilog Assertions, Constrained Random Testing, UVM basics
- **EDA & Tools:** Xilinx Vivado, EDA Playground, Cadence Virtuoso, ModelSim, Proteus, PCB Design Basics
- **Design Domains:** Cryptographic IPs, RISC cores, Traffic Controllers, Signal Routing, Timing-aware FSMs
- **Languages:** Verilog, SystemVerilog, C, Python (for support), Bash (basic), scripting for EDA workflows
- **Traits:** Precision-focused, self-learning RTL builder, understands how hardware + code flow work together

WORK EXPERIENCE

RESEARCH INTERN | Indian Institute of Technology, Madras (IITM) — **March 25- Present**

- Working on an international research project involving web dev, data analysis, visualization, and sensor integration.
- Actively learning and applying necessary tools and skills as part of the research process.

SOC DESIGN AND VERIFICATION INTERN | Tessolve — **July 24- December 24**

- Gained hands-on experience with Verilog/SystemVerilog, advanced verification techniques, and UVM methodologies for efficient design and verification of complex digital systems.
- Designed and verified a cryptographic encryption module using the AES encryption algorithm, achieving high test coverage through Verilog-based testbench development.

PROJECTS

8-Bit RISC Processor | Verilog, SystemVerilog, Vivado — **January 25- February 2025**

- Designed an 8-bit RISC processor with custom ISA, ALU, memory, and control logic using Verilog and RTL design.
- Verified processor functionality with a SystemVerilog testbench and simulated in Vivado (XSIM) for debugging.

Traffic Light Controller | Verilog, FSM, Vivado — **November 24- December 2024**

- Implemented a FSM-based traffic light controller with state transitions, timing control, and LED sequencing using Verilog.
- Simulated and verified design in Vivado (XSIM) for correctness, efficiency, and low power usage.

Cryptographic Accelerator | Verilog, EDA Playground, Vivado, Pipelining — **September 24- November 2024**

- Developed AES-256 cryptographic accelerator using Verilog for FPGA/ASIC with enhanced encryption performance.
- Optimized encryption speed and power efficiency using parallelism, pipelining, and key scheduling techniques.

Smart Shopping Cart | Arduino C, Arduino Uno, IR Sensor, RFID, Servo, OLED display — **February 24- April 2024**

- Designed a smart shopping cart with OLED interface, BO motors, IR sensors, and RFID for autonomous shopping.
- Utilized Arduino UNO and a robotic arm with servo motors for advanced product handling.

CERTIFICATES AND COURSES

SOC Verification using System Verilog | TARAS Systems and Solutions — **July 2024**

- Learned to verify SoC designs using SystemVerilog, focusing on functional, performance, and error detection testing.
- Applied advanced verification techniques like constrained random testing and assertions to ensure SoC design accuracy and reliability.

Embedded Systems and IoT | Tessolve — **February 2024**

- Gained practical skills in embedded systems design and real-time IoT applications integration and got hands-on experience with the MSP430 Board from Texas Instruments.
- Developed IoT solutions using sensors, communication protocols, and embedded systems for industry-specific challenges.

ADDITIONAL HIGHLIGHTS

- Led *Design-A-Thon '24* event in my college with a 4-member team — handled event planning, logistics, and coordination.
- Mentored juniors in career guidance and project planning, including guidance on hosting, uptime, and debugging errors.
- Built 10+ mini-projects — several with a focus on automation, reliability, and system-like responsiveness.
- Built RTL mini-projects including ALUs, MUXes, FSMs, RISC CPUs, and AES blocks with testbenches.
- Self-learned SystemVerilog and verification flow through simulation platforms and hands-on modules.
- Keen on exploring ASIC-level backend and pursuing VLSI roles that blend logic, design, and automation.