Murali Krishna L

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Dear Reader,

I'm Murali — a builder at heart who loves working at the logic level, designing reliable digital systems from the ground up, and verifying that every signal behaves exactly as expected. Thanks for exploring my work — RTL design and SoC verification are where my engineering principles meet real hardware behavior.

Though early in my journey, I've done more than coursework. I've designed an 8-bit RISC processor in Verilog with ALU, register file, control logic, and memory — verified through SystemVerilog testbenches and simulated using Vivado (XSIM). I've also created FSM-based traffic controllers, AES crypto accelerators, Wallace Tree multipliers, and even a missile guidance chip prototype — all RTL-level builds simulated and debugged in Vivado.

At Tessolve, I gained hands-on exposure to SoC-level verification using SystemVerilog and advanced verification techniques like constrained-random testing and assertions. I worked on verifying a 128-bit AES crypto module — building reusable, modular testbenches and monitoring coverage.

My toolbox includes Verilog, SystemVerilog, Vivado, ModelSim, EDA Playground, and solid fundamentals in digital logic design. I've worked with UART, FSMs, mux trees, and hierarchical RTL structures. I've also explored integrating these systems into embedded flows using Proteus and simulation-based development.

Beyond RTL, I'm constantly:

- Revisiting pipelining, hazard handling, and modular ISA design.
- Simulating complex FSM transitions and optimizing logic paths.
- Exploring the intersection of embedded systems and VLSI logic.

What excites me about RTL and DV is the rigor it demands — timing matters, logic matters, and correctness is everything. I may be new, but I'm driven to learn deeper, simulate smarter, and build logic that stands the test.

Thanks for considering my profile — looking forward to contributing meaningfully.

Warm regards,

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